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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF APPEALS

In re Patent Application of: **ROCHE**	Examiner: **K. ABRISHAMKAR**
Serial No. **09/479,105**	Art Unit: **2131**
Confirmation No. **2645**	Attorney Docket No. **99RO21654163**
Filing Date: **JANUARY 7, 2000**	
For: **MICROPROCESSOR WITH PROTECTION CIRCUITS TO SECURE THE ACCESS TO ITS REGISTERS**	

APPELLANT'S APPEAL BRIEF

MS Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Submitted herewith is Appellant's Appeal Brief together with the requisite $500.00 large entity fee for filing a brief. If any additional extension and/or fee is required, authorization is given to charge Deposit Account No. **01-0484.**

(1) Real Party in Interest

The real party in interest is STMicroelectronics, SA, assignee of the present application as recorded at reel 010733, frame 0214.

(2) Related Appeals and Interferences

At present there are no related appeals or interferences.

(3) Status of the Claims

Claims 10-42 are pending in the application, all of which being appealed herein.

(4) Status of the Amendments

All amendments have been entered and there are no further pending amendments. A copy of the claims involved in this appeal is attached hereto as Appendix A.

(5) Summary of the Claimed Subject Matter

Independent Claim 10, for example, is directed to a microprocessor comprising an address bus, a data bus, a plurality of read and write accessible registers **3** connected to the data bus, and an address decoder **2** connected to the address bus for selecting the plurality of registers **3** as a function of an address provided by the address bus. The microprocessor further comprises a plurality of protection circuits **1** connected between the address decoder **2** and the plurality of registers **3**. Each protection circuit **1** is associated with a register **3** to secure access thereto by blocking selection of the register **3** after each resetting of the microprocessor. The protection circuit **1** is released by a successive sending on the data bus N passwords

proper to the register **3** during N first operations for selection of the register **3**, with N≥1. The selection of the associated register **3** is effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor. Independent Claim 37 is a method counterpart of Claim 10. See page 4 line 6 through page 5, line 2, and FIG. 1 reproduced below.

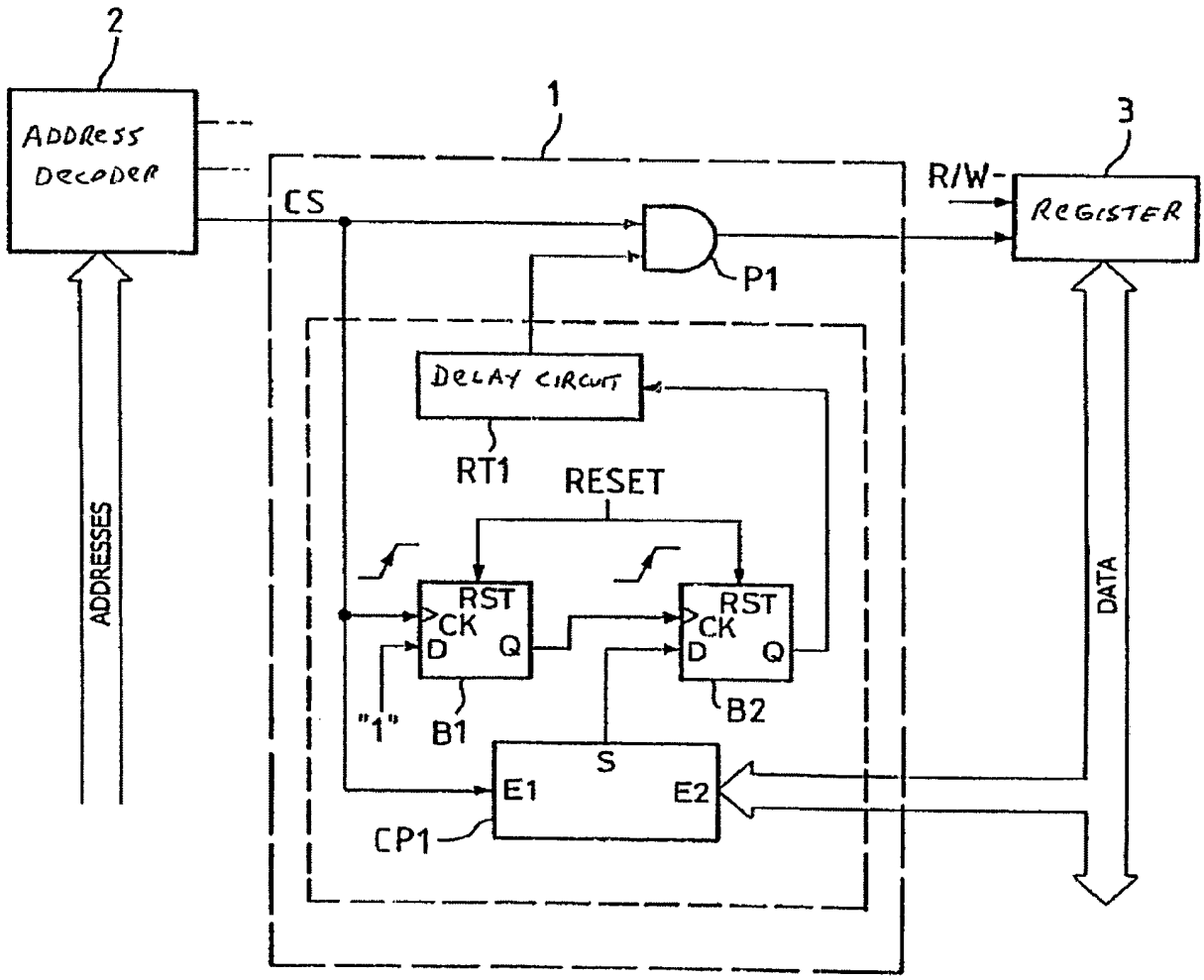

FIG. 1

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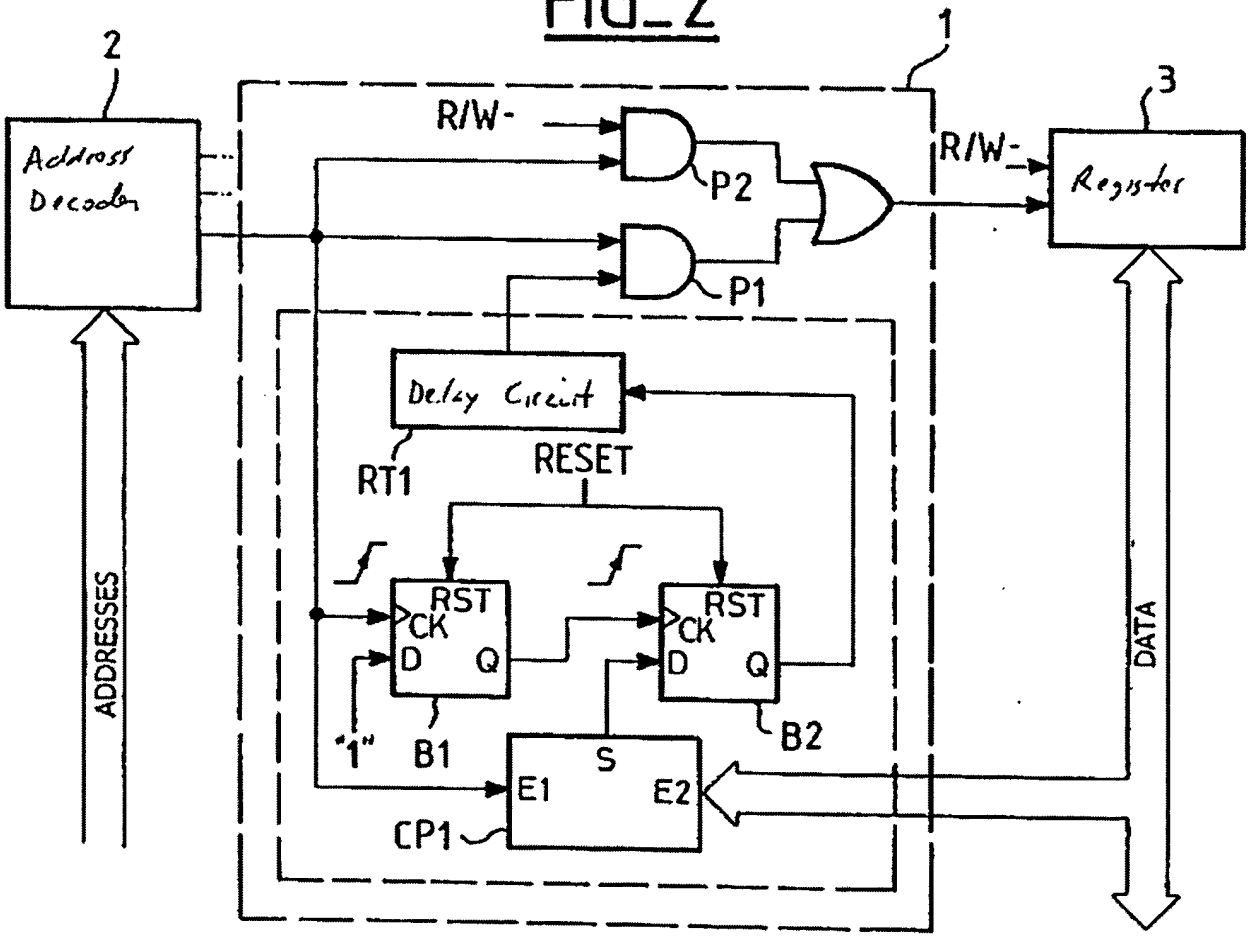
Independent Claim 19 is directed to a microprocessor comprising an address bus, a data bus, a plurality of read and write accessible registers **3** connected to the data bus, and an address decoder **2** connected to the address bus for selecting the plurality of registers **3** as a function of an address provided by the address bus. The microprocessor further comprises a plurality of protection circuits **1** connected between the address decoder **2** and the plurality of registers **3**. Each protection circuit **1** is associated with a register **3** to secure access thereto by blocking selection of the register **3** during write access operations after each resetting of the microprocessor, and releasing of the protection circuit **1** by a successive sending on the data bus of N passwords proper to the register **1** during N first operations for selection of the register **1** with $N \geq 1$, the selection of the associated register **1** being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor. See page 7, line 21 through page 8, line 2, and FIG. 2 reproduced below.

FIG_2



Independent Claim 26 is directed to a microprocessor comprising an address bus, a data bus, a plurality of read and write accessible registers **3** connected to the data bus, and an address decoder **2** connected to the address bus for selecting the plurality of registers **3** as a function of an address provided by the address bus. The microprocessor further comprises a plurality of protection circuits **1** connected between the address

decoder **2** and the plurality of registers **3**. Each protection circuit **1** is associated with a register **3** to secure access thereto by blocking selection of the register **3** after each resetting of the microprocessor, at least two passwords are provided to each register **3**, and releasing of the protection circuit **1** by a successive sending on the data bus of at least 2N passwords proper to the register **3** during N first operations for selection of the register **3** with $N \geq 1$, the selection of the associated register **3** being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor. See page 9, line 8 through page 10, line 8, and FIG. 4 reproduced below.

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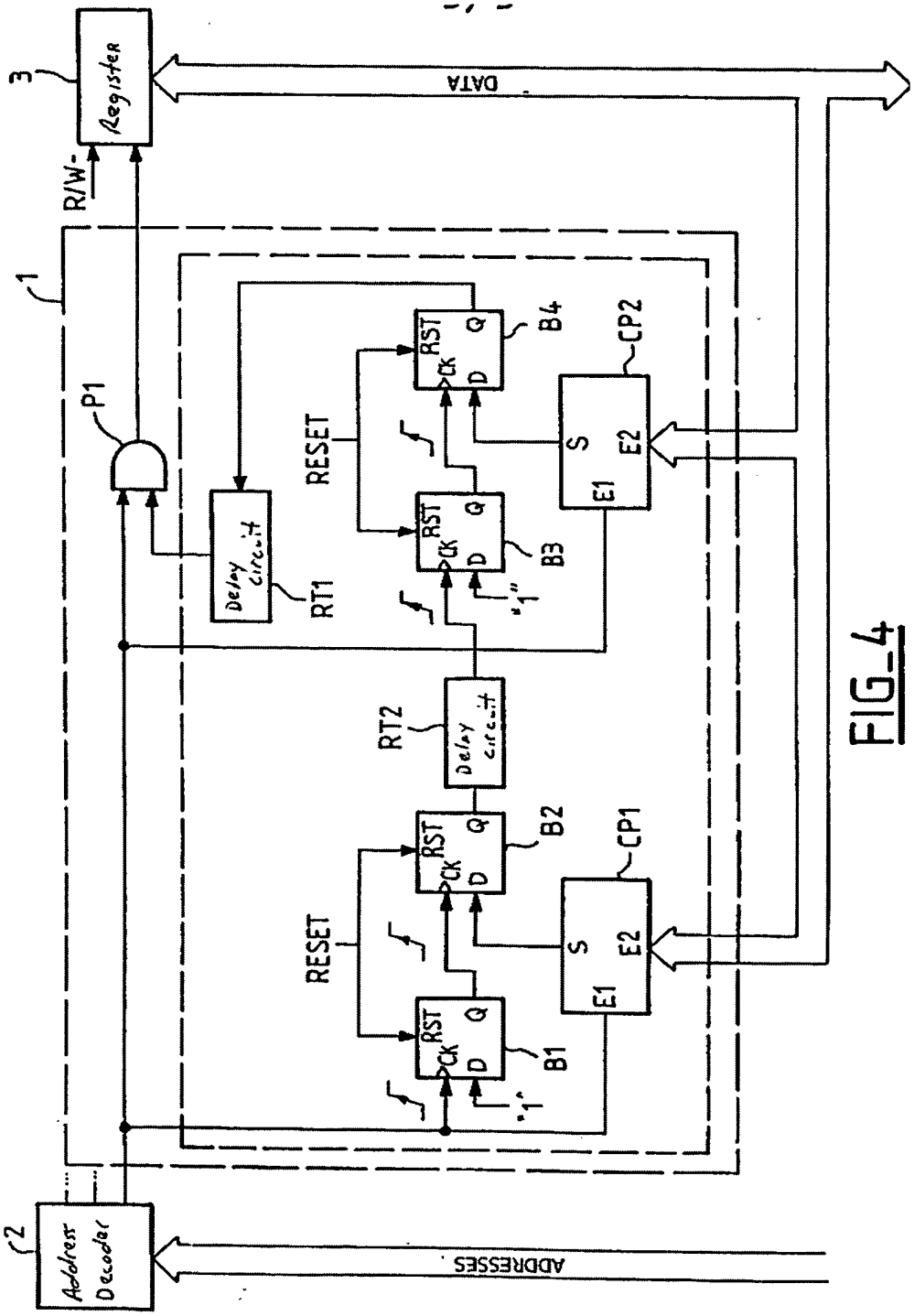

FIG_4

(6) Grounds of Rejection to be Reviewed On Appeal

Claims 10-15, 17-22, 24-32, and 35-42 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over U.S. Patent No. 5,680,581 to Banno et al. Claims 16-18, 23-25, and 33-36 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,680,581 to Banno et al. in view of U.S. Patent No. 5,222,001 to Tokumatsu et al.

(7) Argument

As will be described in greater detail below, Applicant respectfully submits that the Banno et al. patent fails to disclose each and every recitation of the claimed invention.

A. The Claims Are Patentable

As noted above, the Examiner rejected independent Claims 10, 19, 26, and 37 as unpatentable over the Banno et al. patent. The Examiner correctly notes that the Banno et al. patent discloses at column 4, lines 48-55, and in FIGS. 1 and 2, an address bus **15**, a data bus **16**, and an internal program memory read protection circuit **12** comprising an address decoder **12a** connected to the address bus **15**, a memory element **12b**, and an AND gate **12c**.

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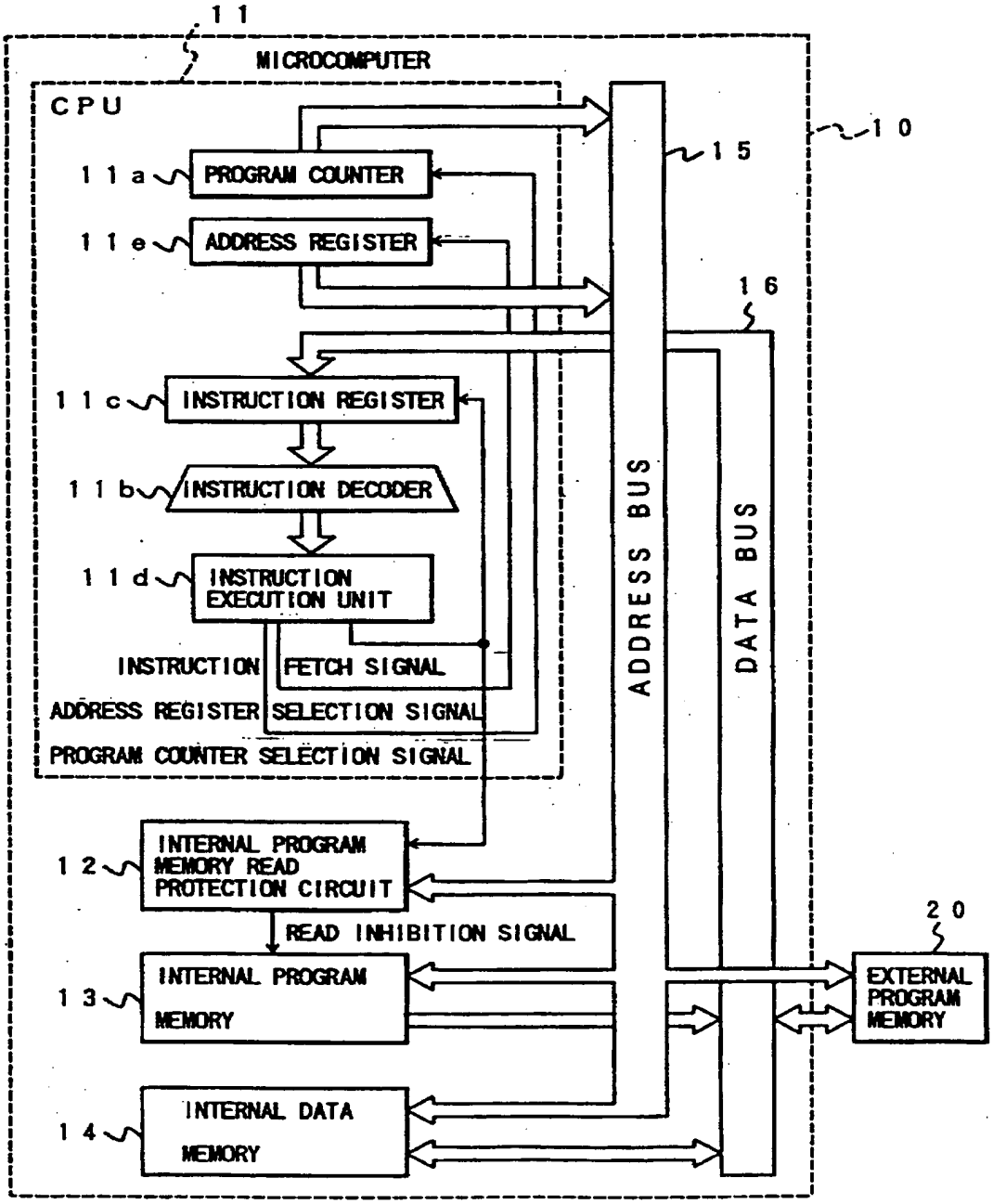

FIG. 1 of Banno et al.

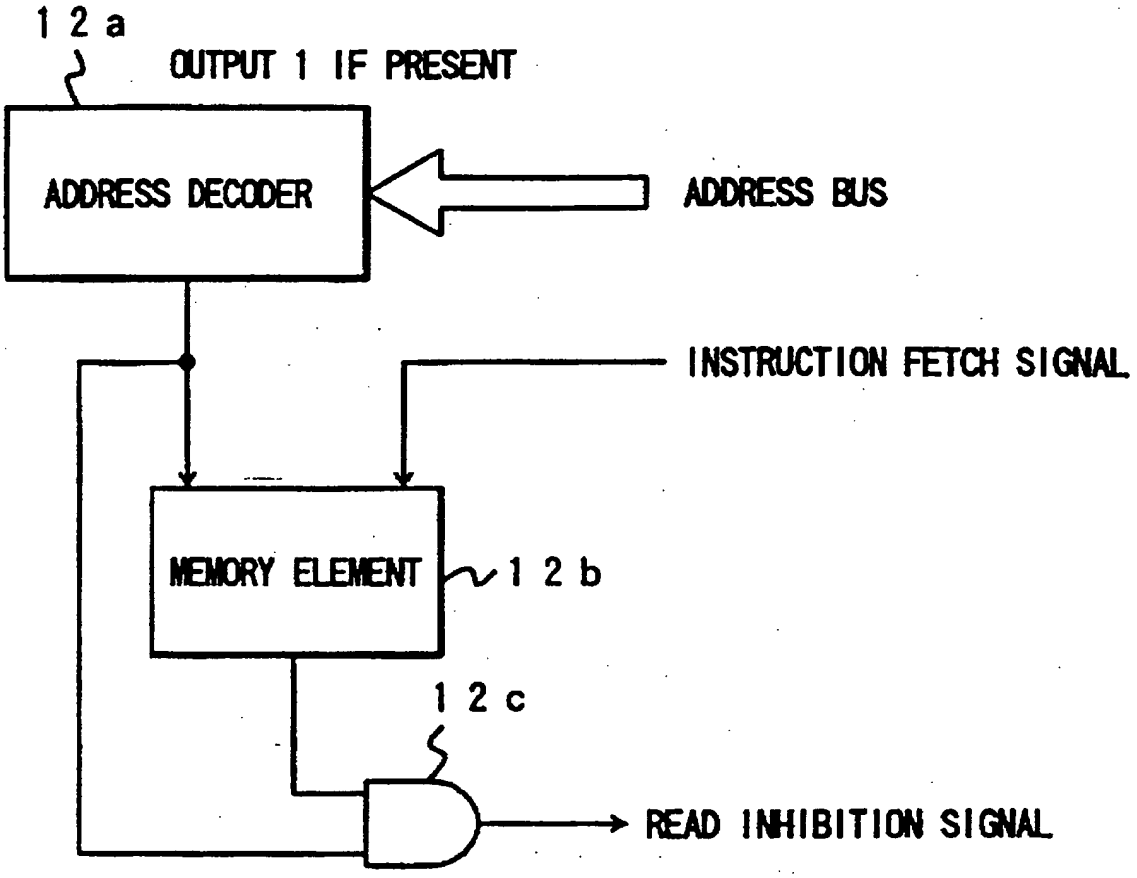

FIG. 2 of Banno et al.

In contrast, independent Claim 10, for example, recites an address bus, a data bus, and a plurality of read and write accessible registers connected to the data bus. In other words, the address bus and data bus are two separate claim elements. Further, the claim recites a protection circuit associated with a register for securing access thereto by blocking selection of the register, and the protection circuit is released by a successive sending on the data bus of N passwords proper to the register.

The claimed protection circuit is therefore responsive to a password sent on the data bus.

The Banno et al. patent fails to disclose such because the internal program memory read protection circuit **12** is responsive to the address bus **15**, not the data bus **16**. For example, in the Banno et al. patent, read access is denied whenever an address of the instruction, which is sent over the address bus **15**, is not present in the address space of the internal program memory **13** thereby triggering the protection circuit **12** as described at column 3, lines 52-57. Independent Claims 19, 26, and 37 include recitations similar to Claim 10.

Accordingly, independent Claims 10, 19, 26, and 37 are patentable. Their dependent claims, which recite yet further distinguishing features, are also patentable over the prior art and require no further discussion herein.

CONCLUSIONS

In view of the foregoing arguments, it is submitted that all of the claims are patentable over the prior art. Accordingly, the Board of Patent Appeals and Interferences is respectfully requested to reverse the earlier unfavorable decision by the Examiner.

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Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: MS Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 5th day of December, 2005.

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APPENDIX A - CLAIMS ON APPEAL
FOR U.S. PATENT APPLICATION SERIAL NO. 09/479,105

Claims 1-9 (Cancelled).

10. A microprocessor comprising:

an address bus;

a data bus;

a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

11. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of

said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

12. A microprocessor according to Claim 10, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor.

13. A microprocessor according to Claim 10, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

14. A microprocessor according to Claim 10, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

15. A microprocessor according to Claim 10, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register if the output signal indicates that the data present on said data bus during the first operation of selection of said register corresponds to the password associated with said register.

16. A microprocessor according to Claim 15, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of said address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said

comparator circuit until the next resetting of the microprocessor.

17. A microprocessor according to Claim 16, wherein said second means comprises:

a delay circuit;

a two-input AND logic gate having a first input connected to the output of said address decoder for selecting the register associated with said protection circuit, a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

18. A microprocessor according to Claim 17, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

19. A microprocessor comprising:

an address bus;

a data bus;

a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers, each protection circuit associated with a register to secure access thereto by blocking selection of said register during write access operations after each resetting of the microprocessor, and releasing of said protection circuit by a successive sending on said data bus of N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

20. A microprocessor according to Claim 19, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

21. A microprocessor according to Claim 19, wherein each protection circuit, during the N first operations for the selection of said associated register, compares N data elements present on said data bus with the N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

22. A microprocessor according to Claim 19, wherein a single password is provided for each register; and wherein each protection circuit comprises:

a comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with the password proper to said register and for delivery of an output signal representing a result of the comparison;

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

second means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection of the register corresponds to the password associated with said register.

23. A microprocessor according to Claim 22, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

24. A microprocessor according to Claim 23, wherein said second means comprises:

a delay circuit;

a first two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input connected through said delay circuit to the output of said second flip-flop circuit of said first means;

a second two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection circuit, and a second input receiving a read/write signal; and

an OR logic gate having a first input connected to an output of said first two-input AND logic gate, and a second input connected to an output of said second two-input AND logic gate, and an output connected to said register.

25. A microprocessor according to Claim 24, wherein said delay circuit comprises a shift register synchronized with the operations for the selection of said associated register.

26. A microprocessor comprising:

an address bus;

a data bus;

a plurality of read and write accessible registers connected to said data bus;

an address decoder connected to said address bus for selecting said plurality of registers as a function of an address provided by said address bus; and

a plurality of protection circuits connected between said address decoder and said plurality of registers;

each protection circuit associated with a register to secure access thereto by blocking selection of said register after each resetting of the microprocessor, at least two passwords are provided to each register, and releasing of said protection circuit by a successive sending on said data bus of at least 2N passwords proper to said register during N first operations for selection of said register with $N \geq 1$, the selection of said associated register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

27. A microprocessor according to Claim 26, wherein the at least two passwords for said associated register are provided over said data bus in a predetermined order.

28. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during read and write access operations to said associated register after each resetting of the microprocessor.

29. A microprocessor according to Claim 26, wherein each protection circuit is arranged to block the selection of said associated register during write access operations to said associated register after each resetting of the microprocessor.

30. A microprocessor according to Claim 26, wherein each protection circuit is connected between an output of said address decoder and a selection input of said associated register for selection thereof.

31. A microprocessor according to Claim 26, wherein each protection circuit, during the N first operations for the selection of said associated register, compare at least 2N data elements present on said data bus with the at least 2N passwords proper to said associated register, and each protection circuit is released for subsequent operations of selection of said

associated register up to the next resetting of the microprocessor if the at least 2N data elements correspond to the at least 2N passwords.

32. A microprocessor according to Claim 26, wherein each protection circuit comprises:

a first protection circuit portion comprising

a first comparator circuit for comparing, during a first operation for the selection of said register, a data element present on said data bus with a first one the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison, and

first means for holding in each protection circuit the output signal until the next resetting of the microprocessor; and

a second protection circuit portion connected to an output of said first protection circuit portion and comprising

a second comparator circuit for comparing, during the first operation for the selection of said register, the data element present on said data bus with a second one of the at least two passwords proper to said register and for delivery of an output signal representing a result of the comparison,

second means for holding in each protection circuit the output signal until the next resetting of the microprocessor, and

third means permitting the selection of said register for the subsequent selection operations of said register if the output signal indicates that the data present on said data bus during the first operation of selection thereof corresponds to the at least two passwords associated with said register.

33. A microprocessor according to Claim 32, wherein said first means comprises first and second D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said first flip-flop circuit having the clock input connected to the output of the address decoder responsible for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal;

said second flip-flop circuit having the clock input connected to the output of said first flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an signal output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor; and

a first delay circuit connected to the output of said second flip-flop circuit.

34. A microprocessor according to Claim 33, wherein said second means comprises third and fourth D type flip-flop circuits, each flip-flop circuit having a clock input, a signal input, a resetting input to which a signal for resetting the microprocessor is applied, and an output;

said third flip-flop circuit having the clock input connected to the output of said first delay circuit for selecting said register associated with said protection circuit, and the signal input for receiving a signal corresponding to a logic signal; and

said fourth flip-flop circuit having the clock input connected to the signal output of said third flip-flop circuit, the signal input for receiving the output signal of said comparator circuit, and an output which delivers the output signal of said comparator circuit until the next resetting of the microprocessor.

35. A microprocessor according to Claim 34, wherein said third means comprises:

a second delay circuit; and

a two-input AND logic gate having a first input connected to the output of said address decoder which has the task of selecting the register associated with said protection

circuit, a second input connected through said second delay circuit to the output of said fourth flip-flop circuit of said first means, and an output connected to the selection input of said associated register.

36. A microprocessor according to Claim 35, wherein said first and second delay circuits each comprises a shift register synchronized with the operations for the selection of said associated register.

37. A method for securing access to a plurality of registers of a microprocessor, the method comprising the steps of:

selecting one of said plurality of registers via an address decoder as a function of an address provided by an address bus connected to the address decoder;

blocking selection of the plurality of registers via a plurality of protection circuits after each resetting of the microprocessor; and

releasing a protection circuit associated with a selected register by successive sending on the data bus N passwords proper to the selected register during N first operations for selection of the register with $N \geq 1$, the selection of the register being effective only for subsequent operations for the selection thereof until a next resetting of the microprocessor.

38. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during read and write access operations to that register after each resetting of the microprocessor.

39. A method according to Claim 37, wherein the step of blocking comprises blocking selection of a selected register during write access operations to that register after each resetting of the microprocessor.

40. A method according to Claim 37, wherein each protection circuit is connected between an output of the address decoder and a selection input of an associated register for selection thereof.

41. A method according to Claim 37, wherein each protection circuit, during the N first operations for the selection of an associated register, compares N data elements present on the data bus with the N passwords proper to the associated register, and each protection circuit is released for subsequent operations of selection of the associated register until the next resetting of the microprocessor if the N data elements correspond to the N passwords.

42. A method according to Claim 37, wherein a single password is provided for each register; and wherein the steps of blocking and releasing comprises:

comparing, during a first operation for the selection of the register, a data element present on the data bus with the password proper to the register and for delivery of an output signal representing a result of the comparison;

holding in each protection circuit the output signal until the next resetting of the microprocessor; and

permitting the selection of the register for the subsequent selection operations of the register if the output signal indicates that the data present on the data bus during the first operation of selection of the register corresponds to the password associated with the register.

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APPENDIX B - OTHER EVIDENCE
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None.

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APPENDIX C - RELATED PROCEEDINGS
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None.